(c) removing upper parts of the oxide films so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region; and

(d) annealing the oxide films, after said removing, at a substrate temperature which is greater than or equal to 1150°C but less than or equal to 1350°C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is less than 1 μm^{-2}.

10. (Amended) The method of claim 9, wherein the organic silicon based CVD method is any of atmospheric pressure CVD method, low pressure CVD method, plasma CVD method, photo CVD method, and liquid phase CVD method.

11. (Amended) The method of claim 9, wherein the annealing is carried out in any one of reductive gas such as H_2 ~~insert~~ inert gas such as He, Ne, AR, Kr, or Xe, O_2, N_2, HCl, CO, and CO_2, or in a gas mixture consisting of any mixture of two kinds of gas selected from these gases.

25. (Twice Amended) A method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions, comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) depositing oxide films in the grooves by an organic silicon based CVD method;

(c) annealing the oxide films at a substrate temperature which is greater than or equal to 1150°C but less than or equal to 1350°C so the dislocation density generated in the semiconductor substrate in a vicinity of the grooves is less than 1 μm^{-2}; and

(d) removing upper parts of the oxide films, after said annealing, so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are

substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region.

26. (Twice Amended) A method of manufacturing a semiconductor substrate having shallow trench isolation, comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) burying oxide films in the grooves by an organic silicon based CVD method; and

(c) annealing said oxide films at a substrate temperature which is greater than or equal to 1150°C but less than or equal to 1350°C so that said oxide films include higher order ring structures higher than 5-fold ring and lower order ring structures lower than 4-fold ring at respective predetermined rates, and an etching rate by ammonium fluoride solution of said oxide films is less than 130 nm/min, which is substantially identical to that of a thermal oxide film.

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27. (Twice Amended) A method of manufacturing a semiconductor substrate having shallow trench isolation, comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) burying oxide films in the grooves by an organic silicon based CVD method; and

(c) annealing the oxide films at a substrate temperature which is greater than or equal to 1150°C, but less than or equal to 1350°C so that said oxide films include higher order ring structures higher than 5-fold ring and lower order ring structures lower than 4-fold ring at respective predetermined rates, the respective predetermined rates of the ring structures are determined according to rates of integrated Raman intensities corresponding to respective ring structures to a total integrated Raman intensity, and the ring structures are formed to satisfy either of or both conditions that said higher order ring structures are substantially

more than 85% of an overall ring structure and said lower order ring structures are substantially less than 15% of the overall ring structure.

28. (Twice Amended) A method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions, comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) forming thin thermal oxidation films on the inner walls of the grooves;

(c) depositing oxide films directly on the thin thermal oxidation films by an organic silicon based CVD method;

(d) removing upper parts of the oxide films so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region; and

(e) annealing the oxide films, after said removing, at a substrate temperature which is greater than or equal to 1150°C but less than or equal to 1350°C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is less than 1 μm^{-2}.

29. (Twice Amended) A method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions, comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) forming thin thermal oxidation films on the inner walls of the grooves;

(c) depositing oxide films directly on the thin thermal oxidation films by an organic silicon based CVD method;

(d) annealing the oxide films at a substrate temperature which is greater than or equal to 1150°C but less than or equal to 1350°C so that dislocation density generated in the semiconductor substrate in a vicinity of the grooves is less than 1 μm^{-2}; and

(e) removing upper parts of the oxide films, after said annealing, so as to planarize a surface of the resulting structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region.

Please add new Claims 30-53 as follows:

30. (New) The method of claim 9, wherein said oxide films are deposited in the grooves so as not to include any nitride film in the grooves.

31. (New) The method of claim 25, wherein said oxide films are deposited in the grooves so as not to include any nitride film in the grooves.

32. (New) The method of claim 26, wherein said oxide films are buried in the grooves so as not to include any nitride film in the grooves.

33. (New) The method of claim 27, wherein said oxide films are buried in the grooves so as not to include any nitride film in the grooves.

34. (New) The method of claim 28, wherein said thin thermal oxidation films are formed by thermally oxidizing inner walls of the grooves.

35. (New) The method of claim 29, wherein said thin thermal oxidation films are formed by thermally oxidizing inner walls of the grooves.

36. (New) A method for forming a microelectronic structure, the method comprising:

(a) forming a mask layer on a substrate wherein the mask layer exposes a part of the substrate;

(b) forming a groove in the exposed part of the substrate;

(c) depositing a layer of an insulating film so as to fill the groove and cover the mask layer;

(d) annealing said insulating film at a temperature which is greater than or equal to 1150°C but less than or equal to 1350°C.

37. (New) The method of claim 36, wherein said annealing is performed for a period of time of about 1 hour to about 2 hours.

38. (New) The method of claim 36, wherein said annealing is performed for a period of time of about 1 hour.

39. (New) The method of claim 36, wherein said annealing is performed in an inert atmosphere.

40. (New) The method of claim 36, wherein said annealing is performed in an atmosphere of nitrogen (N_2).

41. (New) The method of claim 36, further comprising:

planarizing said insulating material so that the substrate is exposed.

42. (New) The method of claim 41, wherein said planarizing comprises using a Chemical Dry Etching (CDE) method.

43. (New) The method of claim 36, wherein said forming the mask layer comprises forming an oxide layer on the substrate.

44. (New) The method of claim 36, wherein said forming the layer of the insulating material comprises forming an oxide layer on inner walls of the groove and depositing an insulating material on the oxide layer to fill the groove.

45. (New) The method of claim 44, wherein said depositing the insulating material comprises forming an oxide by chemical vapor deposition.

46. (New) The method of claim 36, wherein said insulating film is deposited in the groove so as not to include any nitride film in the groove.

47. (New) The method of claim 36, wherein a width of the groove is 0.5 μm.

48. (New) The method of claim 36, wherein said groove tapers.

49. (New) The method of claim 36, wherein said depositing the layer of the insulating film is configured to deposit the insulating film at a thickness larger than a half of a width of the groove.

50. (New) The method of claim 36, wherein said forming the mask is configured to provide a plurality of grooves at a cross sectional view so as to define a SDG region between a couple of the grooves at the cross sectional view.

51. (New) The method of claim 50, wherein said SDG region has a width of 0.3 μm, measured between the couple of the grooves.

52. (New) The method of claim 50, further comprising:

forming source and drain regions in the SDG region sandwiched by the grooves.

53. (New) The method of claim 50, wherein each of the grooves has an aspect ratio d/l_{1x} of less than 10, which is defined by a dimensional ratio of a depth d to a width l_{1x} of an opening at a top of each of the grooves.

REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 9-11 and 14-29 are pending in this application. Claims 16-23 have been withdrawn from consideration. Claims 9-11 and 25-29 have been amended and new Claims 30-53 have been added, all without the introduction of any new matter.